Docket No.: R2180.0159/P159
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kazunari Kimino

Application No.: 10/609,634 Confirmation No.: 4954

Filed: July 1, 2003 Art Unit: 1734

For: APPARATUS AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE Examiner: G. R. Koch

REQUEST FOR RECONSIDERATION
IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The application has been carefully reviewed in light of the rejection dated April 17, 2008. Claims 5, 9, 27, 31, 36, and 39-44 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 41-44 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ciardella I (US 5,711,989). This rejection is respectfully traversed.

Claim 41 recites an apparatus for manufacturing a semiconductor device comprising, *inter alia*, "a substrate holding unit for holding a semiconductor wafer substrate, wherein said semiconductor wafer substrate is provided with at least one electrode formed on a first surface thereof; a discharging mechanism for discharging droplets of raw sealant resin ... onto said first surface of said semiconductor wafer substrate ...; a drive mechanism for displacing at least one of said semiconductor wafer substrate ...; [and] a control unit for controlling said discharging mechanism and said drive mechanism such that said raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode" (emphasis added). Applicant respectfully submits that Ciardella I does not disclose these limitations.

It should be noted that Ciardella I does not contain the cited items. Specifically, on page 2 of the Office Action, a "Figure 5", "chip 10," "solder balls 12" do not appear in Ciardella I. Ciardella I only has figures 1-4. Reference 12 is for a "viscous material dot generator," and reference 10 is for a "rectangular frame." Therefore, the Office Action fails to make a *prima facie* case of anticipation.

Applicant respectfully submits that Ciardella I does not disclose, teach, or suggest that "raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode," as recited in claim 41.

If the Examiner is referring to Bouras (US 5,906,682), which is used in later rejections in the Office Action, and has a "Figure 5", "chip 10," "solder balls 12," it should be noted that Bouras discloses that an epoxy 18 and solder pads 14 completely cover the solder balls 12. FIGs. 2-3; Col. 1, ln. 48-50 and 58-67. Therefore, Bouras also does not disclose the recited limitations.

Since Ciardella I does not disclose all of the limitations of claim 41, claim 41 and dependent claims 42-44 are not anticipated by Ciardella I. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claims 41-44 be withdrawn and the claims allowed.

Claims 36,40, and 41-44 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bouras (US 5,906,682) with reference to Ciardella II (US 5,505,777) (incorporated by reference into Bouras). This rejection is respectfully traversed.

Claims 36 and 40 recite limitations similar to claim 40; therefore, Bouras, even with reference to Ciardella II, does not cure the above-discussed deficiencies of Ciardella I.

To the contrary, Bouras discloses that an epoxy 18 and solder pads 14 completely cover the solder balls 12. FIGs. 2-3; Col. 1, ln. 48-50 and 58-67. Bouras further teaches that "it is desirable that enough liquid epoxy be deposited to encapsulate all of the electrical interconnections and so that a fillet 18a is formed along the side edges of the chip 10." Col. 2, ln. 16-19. This teaches away from leaving a portion of the electrode exposed. Applicant respectfully submits that Bouras does not disclose, teach, or suggest that "raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode," as recited in claims 36, 40, and 41.

Since Bouras (even with Ciardella II) does not disclose all of the limitations of claims 36, 40, and 41, claims 36, 40, and 41 are not anticipated by Bouras. Claims 42-44 depend, respectively, from independent claim 41, and are patentable at least for the reasons mentioned above, and on their own merits. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claims 36,40, and 41-44 be withdrawn and the claims allowed.

Claims 5, 9, 27, and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ciardella I in view of Nakazawa (US 5,935,375). This rejection is respectfully traversed. Claims 5, 9, 27, and 31 recite limitations similar to claim 36; therefore, Nakazawa does not cure the above-discussed deficiencies of Ciardella I. As discussed above, Ciardella I does not contain the cited items. Specifically, on page 2 of the Office Action, a "Figure 5", "chip 10," "solder balls 12" do not appear in Ciardella I. Ciardella I only has figures 1-4. Reference 12 is for a "viscous material dot generator," and reference 10 is for a "rectangular frame." Therefore, the Office Action fails to make a *prima facie* case of anticipation. Nor is Nakazawa cited for these limitations. Thus, Nakazawa does not remedy the deficiencies of Ciardella I.

Since Ciardella I and Nakazawa do not teach or suggest all of the limitations of claims 5, 9, 27, and 31, claims 5, 9, 27, and 31 are not obvious over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, and 31 be withdrawn and the claims allowed.

Claims 36 and 40 stand rejected under 35 U.S.C. § 102(a) as being unpatentable over Ciardella I in view of Bouras. This rejection is respectfully traversed. As discussed above, Bouras discloses that an epoxy 18 and solder pads 14 completely cover the solder balls 12. FIGs. 2-3; Col. 1, ln. 48-50 and 58-67. Bouras further teaches that "it is desirable that enough liquid epoxy be deposited to encapsulate all of the electrical interconnections and so that a fillet 18a is formed along the side edges of the chip 10." Col. 2, ln. 16-19. This teaches away from leaving a portion of the electrode exposed. Applicant respectfully submits that Bouras does not disclose, teach, or suggest that "raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode," as recited in claims 36 and 40. Nor is Ciardella I cited for these limitations.

As discussed above, Ciardella I does not contain the cited items. Thus, Ciardella I does not remedy the deficiencies of Bouras.

Since Bouras and Ciardella I do not teach or suggest all of the limitations of claims 36 and 40, claims 36 and 40 are not obvious over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 36 and 40 be withdrawn and the claims allowed.

Claims 5, 9, 27, and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bouras and Ciardella II in view of Nakazawa. This rejection is respectfully traversed. As discussed above, Bouras discloses that an epoxy 18 and solder pads 14 completely cover the solder balls 12. FIGs. 2-3; Col. 1, ln. 48-50 and 58-67. Bouras further teaches that "it is desirable that enough liquid epoxy be deposited to encapsulate all of the electrical interconnections and so that a fillet 18a is formed along the side edges of the chip 10." Col. 2, ln. 16-19. This teaches away from leaving a portion of the electrode exposed. Applicant respectfully submits that Bouras does not disclose, teach, or suggest that "raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode," as recited in claims 5, 9, 27, and 31. Nor is Nakazawa cited for these limitations. Thus, Nakazawa does not remedy the deficiencies of Bouras.

Since Bouras, Ciardella II, and Nakazawa do not teach or suggest all of the limitations of claims 5, 9, 27, and 31, claims 5, 9, 27, and 31 are not obvious over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, and 31 be withdrawn and the claims allowed.

Claims 5, 9, 27, 31, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ciardella I in view of Prentice (US 6,007,631). This rejection is respectfully traversed. Claim 39 recites limitations similar to claim 5, 9, 27, and 31; therefore, Prentice does not cure the above-discussed deficiencies of Ciardella I. As discussed above, Ciardella I does not contain the cited items. Specifically, on page 2 of the Office Action, a "Figure 5", "chip 10," "solder balls 12" do not appear in Ciardella I. Ciardella I only has figures 1-4. Reference 12 is for a "viscous material dot generator," and reference 10 is for a "rectangular frame." Therefore, the Office Action fails to make a *prima facie* case of anticipation. Nor is Prentice cited for these limitations. Thus, Prentice does not remedy the deficiencies of Ciardella I.

Since Ciardella I and Prentice do not teach or suggest all of the limitations of claims 5, 9, 27, 31, and 39, claims 5, 9, 27, 31, and 39 are not obvious over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, 31, and 39 be withdrawn and the claims allowed.

Claims 5, 9, 27, 31, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bouras and Ciardella II in view of Prentice. This rejection is respectfully traversed. As discussed above, Bouras discloses that an epoxy 18 and solder pads 14 completely cover the solder balls 12. FIGs. 2-3; Col. 1, ln. 48-50 and 58-67. Bouras further teaches that "it is desirable that enough liquid epoxy be deposited to encapsulate all of the electrical interconnections and so that a fillet 18a is formed along the side edges of the chip 10." Col. 2, ln. 16-19. This teaches away from leaving a portion of the electrode exposed. Applicant respectfully submits that Bouras does not disclose, teach, or suggest that "raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode," as recited in claims 5, 9, 27, 31, and 39. Nor

is Prentice cited for these limitations. Thus, Prentice does not remedy the deficiencies of Bouras.

Since Bouras, Ciardella II, and Prentice do not teach or suggest all of the limitations of claims 5, 9, 27, 31, and 39, claims 5, 9, 27, 31, and 39 are not obvious over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, 31, and 39 be withdrawn and the claims allowed.

Claims 5, 9, 27, 31, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ciardella I in view of Cavallaro (US 6,017, 392). This rejection is respectfully traversed. As discussed above, Ciardella I does not contain the cited items. Specifically, on page 2 of the Office Action, a "Figure 5", "chip 10," "solder balls 12" do not appear in Ciardella I. Ciardella I only has figures 1-4. Reference 12 is for a "viscous material dot generator," and reference 10 is for a "rectangular frame." Therefore, the Office Action fails to make a *prima facie* case of anticipation. Nor is Cavallaro cited for these limitations. Thus, Cavallaro does not remedy the deficiencies of Ciardella I.

Since Ciardella I and Cavallaro do not teach or suggest all of the limitations of claims 5, 9, 27, 31, and 39, claims 5, 9, 27, 31, and 39 are not obvious over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, 31, and 39 be withdrawn and the claims allowed.

Claims 5, 9, 27, 31, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bouras and Ciardella II in view of Cavallaro. This rejection is respectfully traversed. As discussed above, Bouras discloses that an epoxy 18 and solder pads 14 completely cover the solder balls 12. FIGs. 2-3; Col. 1, ln. 48-50 and 58-67. Bouras

further teaches that "it is desirable that enough liquid epoxy be deposited to encapsulate all of the electrical interconnections and so that a fillet 18a is formed along the side edges of the chip 10." Col. 2, ln. 16-19. This teaches away from leaving a portion of the electrode exposed. Applicant respectfully submits that Bouras does not disclose, teach, or suggest that "raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode," as recited in claims 5, 9, 27, 31, and 39. Nor is Cavallaro cited for these limitations. Thus, Cavallaro does not remedy the deficiencies of Bouras.

Since Bouras, Ciardella II, and Cavallaro do not teach or suggest all of the limitations of claims 5, 9, 27, 31, and 39, claims 5, 9, 27, 31, and 39 are not obvious over the cited combination. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, 31, and 39 be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: July 16, 2008

Respectfully submitted,

By _____

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